FastFlow: Combining Pattern-Level Abstraction and Efficiency in GPGPUs

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Outline

- Motivational example
  - An effective (and quite universal) image/video denoiser
  - Paradigmatic programming pattern for GPGPUs?
- On patterns for multicore and GPGPUs
  - FastFlow
  - Some performance results
  - A demo
Salt & Pepper noise

- Electronic and signal noise
- Uniform distribution of “saturated” white/black pixels
  - Measured as percentage of affected vs overall pixels
- Typically restored using statistic filters: e.g. median, median-adaptive
- Not satisfactory for high levels of noise
  - not only outliers are filtered (image results smoothed)
Salt & Pepper noise

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Gaussian noise

- Poor illumination, temperature, circuit noise
- White additive noise in the frequency domain
  - Measured with mean and variance of the Gaussian distribution
  - Affect all pixels, with an additive “white” value distributed as a Gaussian
- Typically restored using statistic filters: e.g. median, Gaussian smoothing
- More difficult to manage: restored image results smoothed
Two-stage restoring

- progressive-switching/adaptive median
- neural/bayesian networks, fuzzy, ...
- variational
- statistic

- Decouple detection decoupled from restoration
  - Pixels considered not outliers are not altered by restoration
  - False positives impair restoration quality
Two-stage restoring

- Statistic detection + variational restoration
  - High quality, edge-preserving filtering
  - Much more computational demanding, not really viable without parallelism
    - Matlab on a single 256x256 image with 50% of noise requires dozen of minutes
  - Stages can be pipelined

- progressive-switching/adaptive median
  - neural/bayesian networks, fuzzy, …

- variational
  - statistic
Variational De-noising: an iterative optimisation problem

Try any possible color \( k \) for the pixel, choose \( u \), the one that minimize the value of \( F(\text{neighb8}(i,j)) \)

\( F(\ldots) \) weight differently noisy and not noisy pixels

You can write it directly with C++ and CUDA but what happens splitting the work onto 2 GPGPUs?
Variational Denoise: $F(\ldots)$ details
(almost universal for different noise types)

\[
\arg\min_{u \in N} F(u) = \alpha \int R(u) + \beta \int D(u, d)
\]

In the spatial domain
\[
Fd|_N(u) = \sum_{(i,j) \in N} [|u_{i,j} - d_{i,j}| + \frac{\beta}{2} (S_1 + S_2)]
\]
\[
S_1 = \sum_{(m,n) \in V_{i,j} \cap N} 2 \cdot \varphi(u_{i,j} - d_{m,n})
\]
\[
S_2 = \sum_{(m,n) \in V_{i,j} \cap N^c} \varphi(u_{i,j} - u_{m,n})
\]

\[
\varphi(t) = |t|^\alpha \quad \text{with} \quad 1 < \alpha \leq 2 \quad \text{for Salt&Pepper}
\]

Convergence can’t be evaluated with a reduce (involves three iterations, i.e. memory)

Noisy Img → Img (k-1) → Img (k) → Img (k+1)

Residuals

\[
\begin{array}{ccc}
2 & 4 & 2 \\
5 & 8 & 5 \\
6 & 7 & 6 \\
\end{array}
\]

Diff of residuals

\[
\begin{array}{ccc}
3 & 4 & 3 \\
2 & 4 & 2 \\
5 & 8 & 5 \\
\end{array}
\]

Reduce of diffs

\[
\sum \Delta^{(k)} = 10 \\
\sum \Delta^{(k+1)} = 3 \\
\]

\[
\frac{\|\sum \Delta^{(k)}\| - \|\sum \Delta^{(k+1)}\|}{\|\sum \Delta^{(k)}\|} < \epsilon \in \mathcal{R}
\]
Quality results

Original
Baboon standard
test image
1024x1024

10% impulsive noise

50% impulsive noise

90% impulsive noise

Restored

PNSR 43.29dB MAE 0.35
PNSR 32.75dB MAE 2.67
PNSR 23.4 MAE 11.21
Patterns are a natural approach in GPGPUs

... and this well-known from long time

Think in Parallel

The GPU is a data-parallel processor
- Thousands of parallel threads
- Thousands of data elements to process
- All data processed by the same program
- SPMD computation model
- Contrast with task parallelism and ILP

Best results when you “Think Data Parallel”
- Design your algorithm for data-parallelism
- Understand parallel algorithmic complexity and efficiency
- Use data-parallel algorithmic primitives as building blocks

Data-Parallel Algorithms

Efficient algorithms require efficient building blocks
This talk: data-parallel building blocks
- Map
- Gather & Scatter
- Reduce
- Scan

but are “standard” and “flat”
data-parallel pattern expressive enough for the problems?
Rationale: patterns are there but are not simply map or reduce

- Detect-Denoise can be naturally pipelined
- Denoise is a (sort of) map with a stencil
  - Where, $x = <x_1, x_2, \ldots, x_n>$, map $f(x) = <f(x_1), f(x_2), \ldots, f(x_n)>$
  - Can be written as a map, but is neither natural nor easy
- Convergence evaluation is map across three iterations and reduce
  - Even more complex to write it as a MapReduce (if not impossible)
- Cholesky LU or C4.5 tree pruning with map, reduce or MapReduce?
StencilReduce

- a (low-level) powerful pattern
- it captures most of the interesting data parallel GPGPUs computations
- Subsumes: map, reduce, mapReduce
- Programmers do not need to write any line of host code to drive the GPGPU
- D2H/H2D, data feeding, synchronisations, block configurations, …

Loop

before (...)  
Stencil<stencilK,reduceK> (data[i], env)  
reduce op data  
after (...)
**stencilReduce**

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```python
loop
before (...) stencil<stencilK,reduceK> (data[i], env)
reduce op data
after (...) compute on host
```

Unified Memory greatly simplify this part

CUDA code

Compute on host possibly in parallel on CPU cores

Compute on host possibly in parallel on CPU cores
Low-level approaches = lot of freedom (threads, CUDA, OpenCL, MPI, …)

you can design your algorithms as you want
… as a car, you can drive it where you want

Val D’Orcia, Tuscany, Italy
Low-level approaches = lot of freedom (threads, CUDA, OpenCL, MPI, …)

- Think in parallel & high-level
  - Efficiency, portability, time-to-market
- High-level parallel patterns
  - Describing collective behavior
  - Can be: expressive, efficient, compositional
  - Targeting multicore, GPGPUs, distributed with an unifying vision
  - On various CPUs/GPGPUs and OSes

you can design your algorithms as you want … as a car, you can drive it where you want

Sao Paulo, Brasil
FastFlow (FF)

- C++ header-only library
- Portable everywhere exists a C++ compiler
- Originally designed for high-frequency streaming
- Provides stream-oriented and data-parallel patterns
  - compositional, efficient
- Accommodate diversity
  - if you need a different pattern, do it extending a C++ class
- Multi-core, GPGPUs, distributed
- https://sourceforge.net/projects/mc-fastflow
FF building blocks: nodes and channels

channel name or channel

node

channel names

channel name or channel

mi-node

channel names

channel name or channel

mo-node

threads or processes threads are non-blocking (can be suspended using a native protocol)

FF bound shmem FIFO channel
Single-Producer-Single-Consumer lock-free fence-free queue

FF unbound shmem FIFO channel
Single-Producer-Single-Consumer lock-free fence-free queue

shmem channels communicate pointers in a message passing style

Distributed zero-copy channel
OMQ/TCP or native IB/OFED

MVAPICH ~ 190ns

faster and more scalable than CAS/test-and-set implement.

Master-workers (0.5 μS workload)
Master-workers (5 μS workload)
Master-workers (5 μS workload)
Semantics of the node: dataflow activation

```cpp
class mynode: public ff_node {
public:
    int svc_init() {
        /* after constructor - running as a thread */
        return 0;
    }

    void * svc(void * task) {
        int * t = (mytask_t *) task;
        // do something on task
        cout << "mynode " << ff_node::get_my_id()
            << " received task " << t->payload << "\n";
        return task;
    }

    void svc_end() {
        /* before destructor - running as a thread */
    }
};
```

mynode is created as a standard C++ class extending ff_node
Semantics of the node: dataflow activation

After class construction
mynode is turn into a thread

Nodes are not tasks (as in TBB), they are executors

The svc_init() method is executed

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        return task;
    }

    void svc_end() {
        /* before destructor - running as a thread */
    }
};
```
Semantics of the node: dataflow activation

the node enters in a infinite loop
1. get a task from input channel (i.e. a pointer)
2. execute svc method
3. put a task the output channel (i.e. a pointer)

svc() might output more tasks via
ff_send_out call (not shown)

The node terminate on returning a NULL
pointer

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            << " received task " << t->payload << "\n";
        return task;
    }

    void svc_end() {
        /* before destructor - running as a thread */
    }
};
FF core patterns: pipe, farm, feedback
they are streaming networks, not task graphs

- Pipeline: S1 → S2 → ... → Sn
- Farm: W1 → W2 → ... → Wn
- Feedback: E → W1 → W2 → ... → Wn

or any composition of them (e.g. D&C and Master-Workers)
```cpp
#include <vector>
#include <iostream>
#include <ff/farm.hpp>

using namespace ff;

// generic worker
class Worker: public ff_node {
public:
    void* svc(void* task) {
        int* t = (int*) task;
        std::cout << "Worker " << ff_node::get_my_id() << " received task " << *t << "\n";
        return task;
    }

    // I don't need the following functions for this test
    //int svc_init() { return 0; } //void svc_end() {}
};

// the gatherer filter
class Collector: public ff_node {
public:
    void* svc(void* task) {
        int* t = (int*) task;
        if (*t == -1) return NULL;
        return task;
    }
};

// the load-balancer filter
class Emitter: public ff_node {
public:
    Emitter(int max_task):ntask(max_task) {};
    void* svc(void*) {
        int* task = new int(ntask);
        --ntask;
        if (ntask<0) return NULL;
        return task;
    }

    private:
        int ntask;
};

int main(int argc, char* argv[]) {
    if (argc<3) {
        std::cerr << "use: " << argv[0] << " nworkers streamlen\n";
        return -1;
    }

    int nworkers=atoi(argv[1]);
    int streamlen=atoi(argv[2]);

    if (!nworkers || !streamlen) {
        std::cerr << "Wrong parameters values\n";
        return -1;
    }

    ff_farm<> farm; // farm object
    Emitter E(streamlen);
    farm.add_emitter(&E);

    std::vector<ff_node *> w;
    for(int i=0;i<nworkers;++i) w.push_back(new Worker);
    farm.add_workers(w); // add all workers to the farm
    Collector C;
    farm.add_collector(&C);

    if (farm.run_and_wait_end()<0) {
        error("running farm\n");
        return -1;
    }

    std::cerr << "DONE, time= " << farm.ffTime() << " (ms)\n";
    farm.ffStats(std::cerr);
    return 0;
}
```
GPGPUs

- Fill stencilReduce methods with CUDA kernel code
  - No CUDA-related host code at all need to be written

- Possibly nest stencilReduce into another pattern
  - e.g. farm to use many GPGPUs
    - the async copy engine is automatically used via CUDA streams
  - Helpful to mix threading (or distributed) with GPGPUs
  - If you already have your standard host+CUDA code just copy-paste into a svc( ) method
FF core patterns: rationale

- farm: process in parallel independent tasks (e.g. C++ objects)
  - true dependencies are enforced only along edges of the graph
  - workers might synchronise (e.g. w locks/atomics), synchronisation in the business code
- farm, pipeline and feedback (to build cyclic networks) are enough to write all other patterns
- Think to GPGPUs design
  - They be though as machines to compute a map, reduce, stencil, …
  - … but in hardware they are built as a farm that dispatches independent blocks onto multiprocessors (+global memory)
FF high-level patterns

- Proposed as code annotations
  - Similarly to openMP, openacc, ...
  - used to generate a graph at the core pattern level

- Examples
  - parallel_for
  - map, reduce, MapReduce, ... (targeting GPGPUs)
  - and as many as you want: developing a new pattern is just developing a new class
Example: map (derived from stencilReduce)

- 2 or more GPGPUs on the same platform
  - nest a stencilReduce, map, reduce … into a (host) farm with 2 workers
  - (future: we need to understand how to use NVLINK)

- offload code onto distributed GPGPUs
  - nest a stencilReduce, map, reduce … into a (host) distributed farm with 2 workers
  - data serialisation is up to user, the framework just provides callback to do it

- In both cases
  - be sure that tasks are independent (otherwise you need another pattern)
Example: map (derived from stencilReduce)

```
FFMAPFUNC(mapF, unsigned int, in, return (in * 2););

class cudaTask: public baseCUDATask<unsigned int> {
public:
    void setTask(void* t) {
        if (t) {
            cudaTask *t_ = (cudaTask *) t;
            setInPtr(t_-&in); // match of data pointer H2D
            setOutPtr(t_-&in); // match of data pointer D2H
            setSizeIn(inputsize); // needed without Unified memory
        }
    }

    unsigned int *in, *out;
};

main () {
    ...
    // put the input in task->in
    FFMAPCUDA(cudaTask, mapF) *myMap = new FFMAPCUDA(cudaTask, mapF)(*task);
    myMap->run_and_wait_end();
    // result is in task->out
    ...
}
```
Example: map (derived from stencilReduce)

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class cudaTask: public baseCUDATask<unsigned int> {
public:
    void setTask(void* t) {
        if (t) {
            cudaTask *t_ = (cudaTask *) t;
            setInPtr(t_->in); // match of data pointer H2D
            setOutPtr(t_->in); // match of data pointer D2H
            setSizeIn(inputsize); // needed without Unified memory
        }
    }

    unsigned int *in, *out;
};

main () {
    ...
    // put the input in task->in
    FFMAPCUDA(cudaTask, mapF) *myMap = new FFMAPCUDA(cudaTask, mapF)(*task);
    myMap->run_and_wait_end();
    // result is in task->out
    ...
}
```

This is CUDA code

Simple in this case, but any CUDA code is valid here

It will be compiled with NVCC

This is a macro

For multicore we use C++11 lambda. Theoretically possible to use Lambda for kernel code? (maybe with UnifiedMemory)
GPGPU code: Rationale

- Is it worth abstract even more?
  - In particular, the CUDA code

- No, we believe
  - Often not needed: CUDA code if often C++ code
  - Access to thread_id, always needed
  - Programmers would like to super-optimize their code
    - using all CUDA features
  - CUDA evolves too rapidly
“Demo”

map, farm(map), …
“Demo”
denoiser
Example: Qt-mandelbrot (from Qt samples)

Original (sequential)

```cpp
const int Limit = 4;
bool allBlack = true;
if (restart) break;
if (abort) return;

for (int y = -halfHeight; y < halfHeight; ++y) {
    uint *scanLine = reinterpret_cast<uint *>(image.scanLine(y + halfHeight));
    double ay = centerY + (y * scaleFactor);
}
```

FastFlow (parallel)

```cpp
const int Limit = 4;
bool allBlack = true;
if (restart) break;
if (abort) return;

pf_det.parallel_for(-halfHeight, halfHeight, 1, halfHeight,
[@](const long y) {
    uint *scanLine = reinterpret_cast<uint *>(image.scanLine(y + halfHeight));
    double ay = centerY + (y * scaleFactor);
}
```

private:

```cpp
ParallelFor pf_det;
```
“Demo”

mandelbrot
Performance ( multicore )

Bowtie2 tool (DNA mapping)

Smith-Waterman (SSE2) against OpenMP, Cilk, TBB

Cholesky LU against PLASMA

Original version: pthreads + test&set spinlocks

FF differs no more than 30 lines of code from the original on several thousands (including memory affinity management)
Performance (CPUs + GPGPUs)
Video frames 768x512

Nehalem 32 cores + 1 K20
32 cores + K20
32 core

SandyBridge 16 cores + 2 Tesla M2090
16 cores + 2xM2090
16 cores + 1xM2090
16 cores

no difference w.r.t. hand-written CUDA code
FastFlow: a framework for research

- Open-minded patterns
  - A pattern is missing? Not happy of the implementation? Modify it extending a class …
  - Multicore, GPGPUs, distributed under the same theoretical umbrella. No compilers to modify (!)
  - Non expert programmers does not need to deal with synchronisations and data copies, just select patterns

- Productivity: portability, reduced development time, porting of legacy applications, …

- Comparable or better with OpenMP and TBB on fine grain
  - Comparable with OpenMP on data-parallel - really fast on streaming (especially very high-frequency)

- Entirely C++ (\texttt{C++11}), minimalistic design, solid enough to test new solutions
  - E.g. FastFlow lock-free parallel memory allocator extend with CUDA UnifiedMemory

- Main platform is Linux, but works almost everywhere exist a C++ compiler
  - MacOS, Win — x86, x86_64, Xeon Phi, PPC, Arm, Tilera, NVidia (CUDA and OpenCL) — gcc, clang, icc, nvcc
FastFlow: a framework for research

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Thanks

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https://sourceforge.net/projects/mc-fastflow/